

Application Number 10/714,801
Amendment dated July 24, 2006
Reply to Office Action of May 22, 2006

Amendments to the Claims:

Please amend claims 1, 7, 11, 12 and 17, and cancel claims 6, 8, 10, 16 and 18 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A multi-chip package comprising:

a first semiconductor chip which shows good results when tested for reliability after being assembled at a package level;

at least one second semiconductor chip which is in a wafer level configuration and is stacked on the first semiconductor chip via stacking means, wherein a back surface of the first semiconductor chip [[abuts]]faces a back surface of the second semiconductor chip;

a first connecting unit attached to a surface opposite the back surface of the first semiconductor chip for electrically connecting the first semiconductor chip to an external system; and

a second connecting unit attached to a surface opposite the back surface of the second semiconductor chip for electrically connecting the second semiconductor chip to the external system,

wherein the first connecting unit is different from the second connecting unit, and the first semiconductor chip includes a flash memory.

2. (Previously Presented) The multi-chip package of claim 1, further comprising a printed circuit board for the multi-chip package, which includes bonding pads to which the first connecting unit and the second connecting unit are connected, and pins for connecting the bonding pads to the external system.

3. (Previously Presented) The multi-chip package of claim 2, further comprising a molding compound for fastening the first and second semiconductor chips and protecting the first and second semiconductor chips from the external environment.

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4. (Previously Presented) The multi-chip package of claim 3, wherein the stacking means are an adhesive.

5. (Previously Presented) The multi-chip package of claim 4, wherein a package type of the first semiconductor chip is a Fine Ball Grid Array (FBGA) or a Wafer-Level Chip Size Package (W-CSP).

6. (Cancelled)

7. (Currently Amended) The multi-chip package of claim [[6]]5, wherein a package type of the printed circuit board is a Ball Grid Array (BGA).

8. (Cancelled)

9. (Previously Presented) The multi-chip package of claim 4, wherein a package type of the first semiconductor chip is a Thin Quad Flat package (TQFP) or a Super Thin Small Outline Package (STSOP).

10. (Cancelled)

11. (Currently Amended) The multi-chip package of claim [[10]]9, wherein a package type of the printed circuit board is a BGA.

12. (Currently Amended) The multi-chip package of claim [[10]]9, wherein a package type of the printed circuit board is a TQFP.

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13. (Withdrawn) The stack type multi-chip package of claim 11, wherein one surface, on which pads of the first semiconductor chip are disposed, faces and is stacked on a back surface of the second semiconductor chip via the adhesive.

14. (Withdrawn) The stack type multi-chip package of claim 12, wherein one surface, on which pads of the first semiconductor chip are disposed, faces and is stacked on a back surface of the second semiconductor chip via the adhesive.

15. (Previously Presented) The multi-chip package of claim 4, wherein a package type of the first semiconductor chip is a BGA.

16. (Cancelled)

17. (Currently Amended) The multi-chip package of claim [[16]]15, wherein a package type of the printed circuit board is a TQFP.

18. (Cancelled)